#12 Letter to draft T. re Oath-Brous 4/1/02

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PATENT
EMC-97-060

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICANT:	Reema Gupta, Yao Wang, and Alesia Tringale	*GROUP ART UNIT:*	2154
U.S.S.N.:	09/213,613	*EXAMINER:*	Andrew Caldwell
FILING DATE:	December 18, 1998	*CONFIRMATION NO.*	6656
TITLE:	*MESSAGING MECHANISM FOR INTER PROCESSOR COMMUNICATION*		

Attn.: *Official Draftsperson*
Assistant Commissioner for Patents
Washington, DC 20231

LETTER TO OFFICIAL DRAFTSPERSON

Sir:

Subject to the approval of the Primary Examiner in this case, enclosed for filing are thirty-eight (38) sheets of Formal Drawings, Figures 1-33, labeled, for the above-referenced patent application. Also enclosed is a copy of PTO Form 948, "Notice of Draftsperson's Patent Drawing Review."

Please charge any fees occasioned by this submission to Deposit Account 05-0889.

Respectfully submitted,

Dated:

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G/ChrisG/Prosec/EMC-97-060
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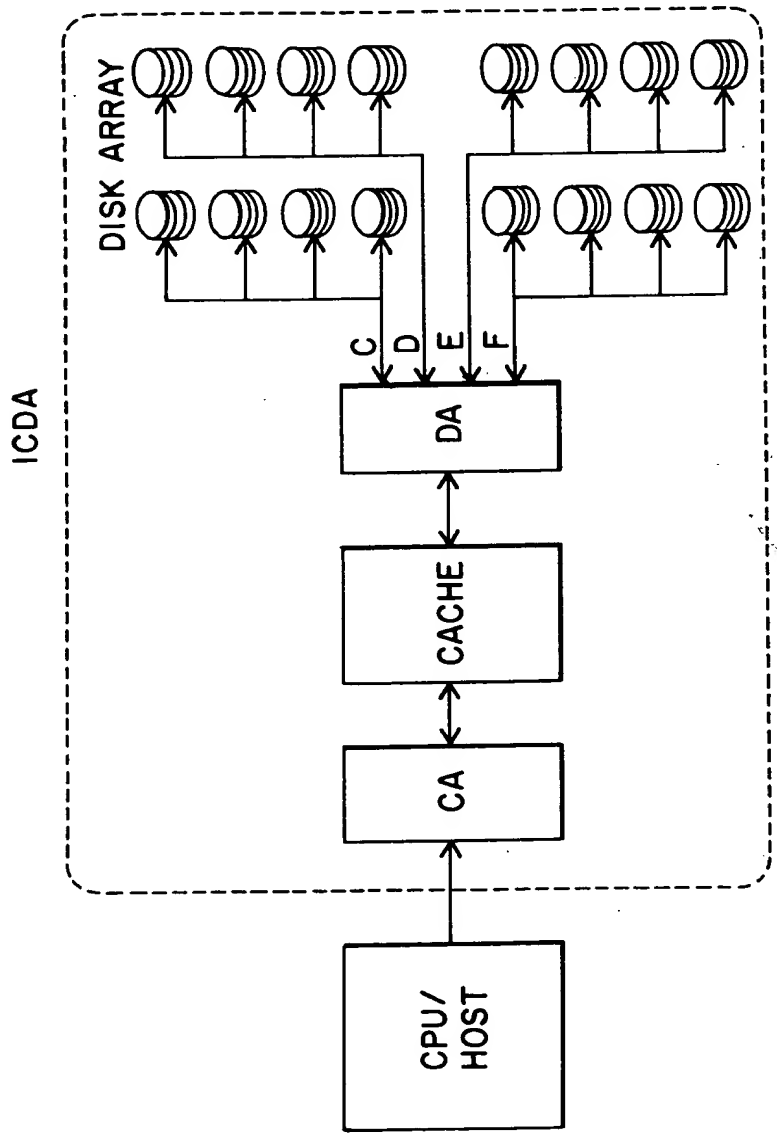


FIG. 1
(PRIOR ART)

ESCON FRONT END
(PRIOR ART)

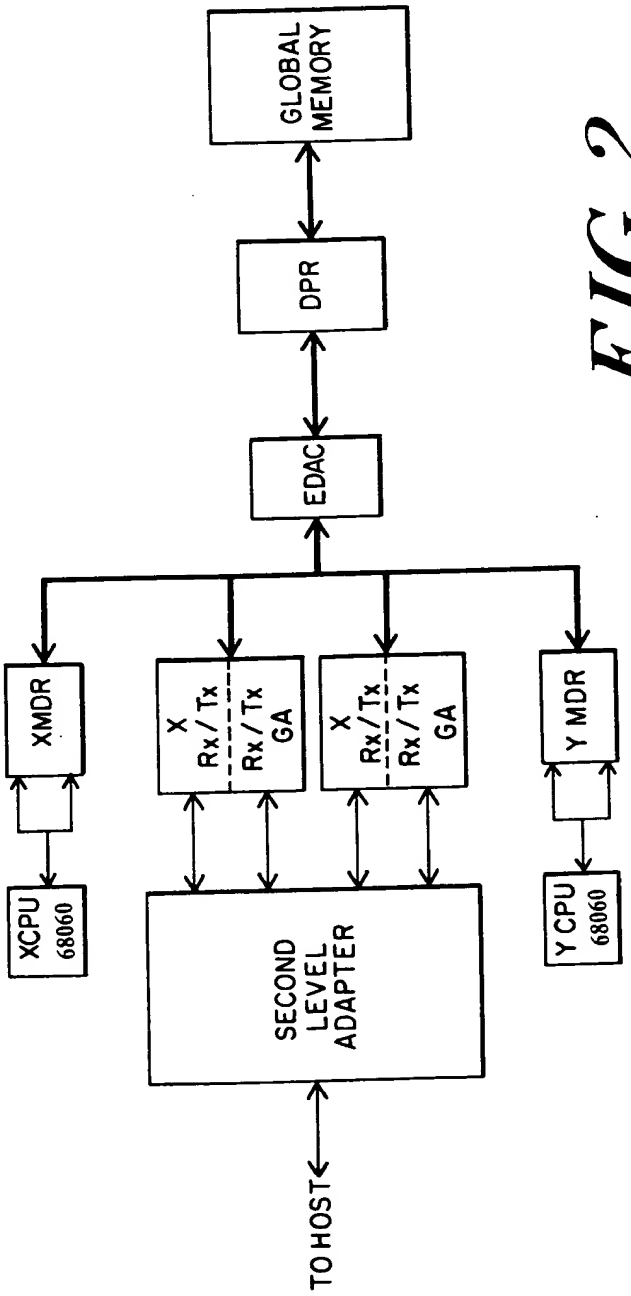


FIG. 2

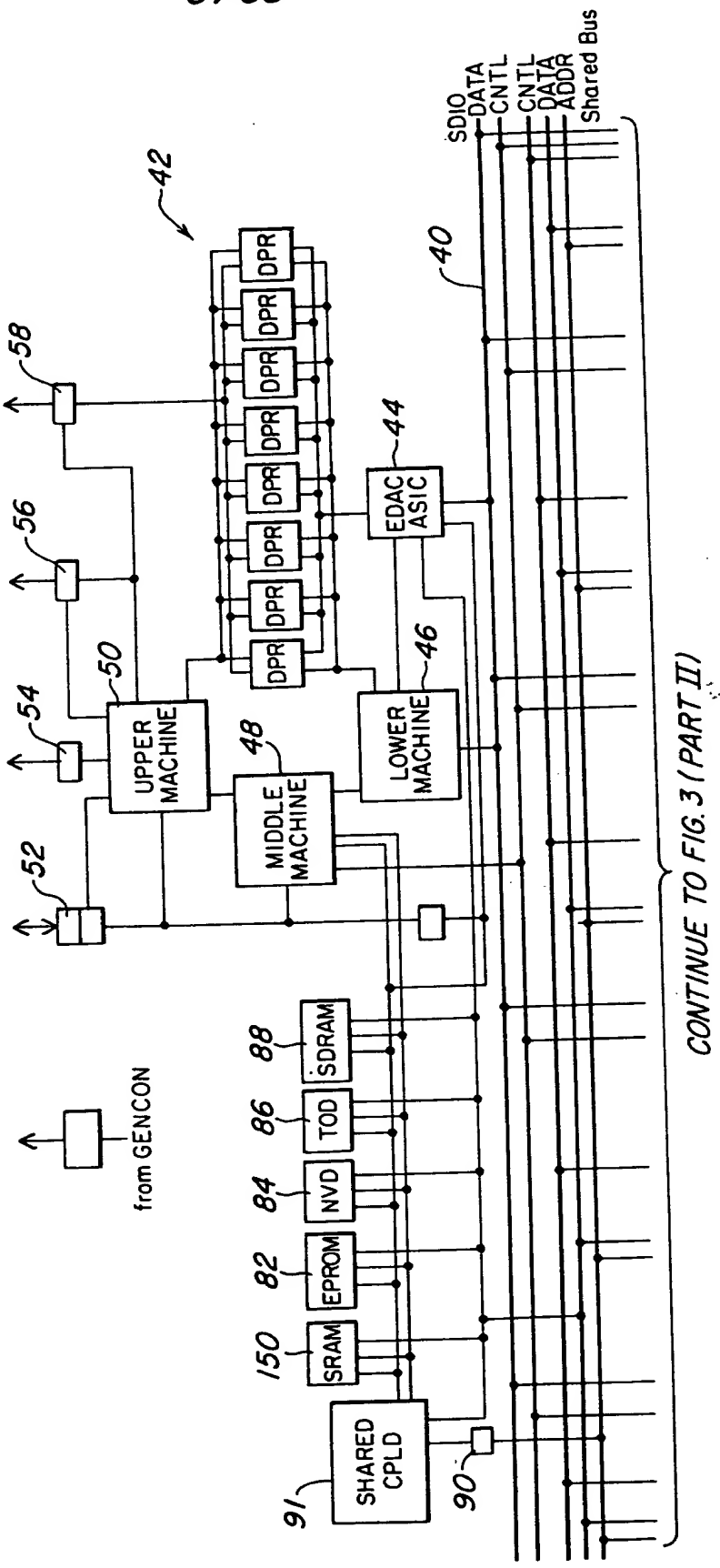

SDIO
DATA
CNTL
CNTL
DATA
ADDR
Shared Bus
42
DPR
DPR
DPR
DPR
DPR
DPR
DPR
DPR
40
58
56
54
52
50
UPPER MACHINE
48
MIDDLE MACHINE
46
LOWER MACHINE
44
EDAC ASIC
from GENCON
88
SDRAM
86
TOD
84
NVD
82
EPROM
150
SRAM
SHARED CPLD
91
90
CONTINUE TO FIG. 3 (PART II)

FIG. 3
(PART I)

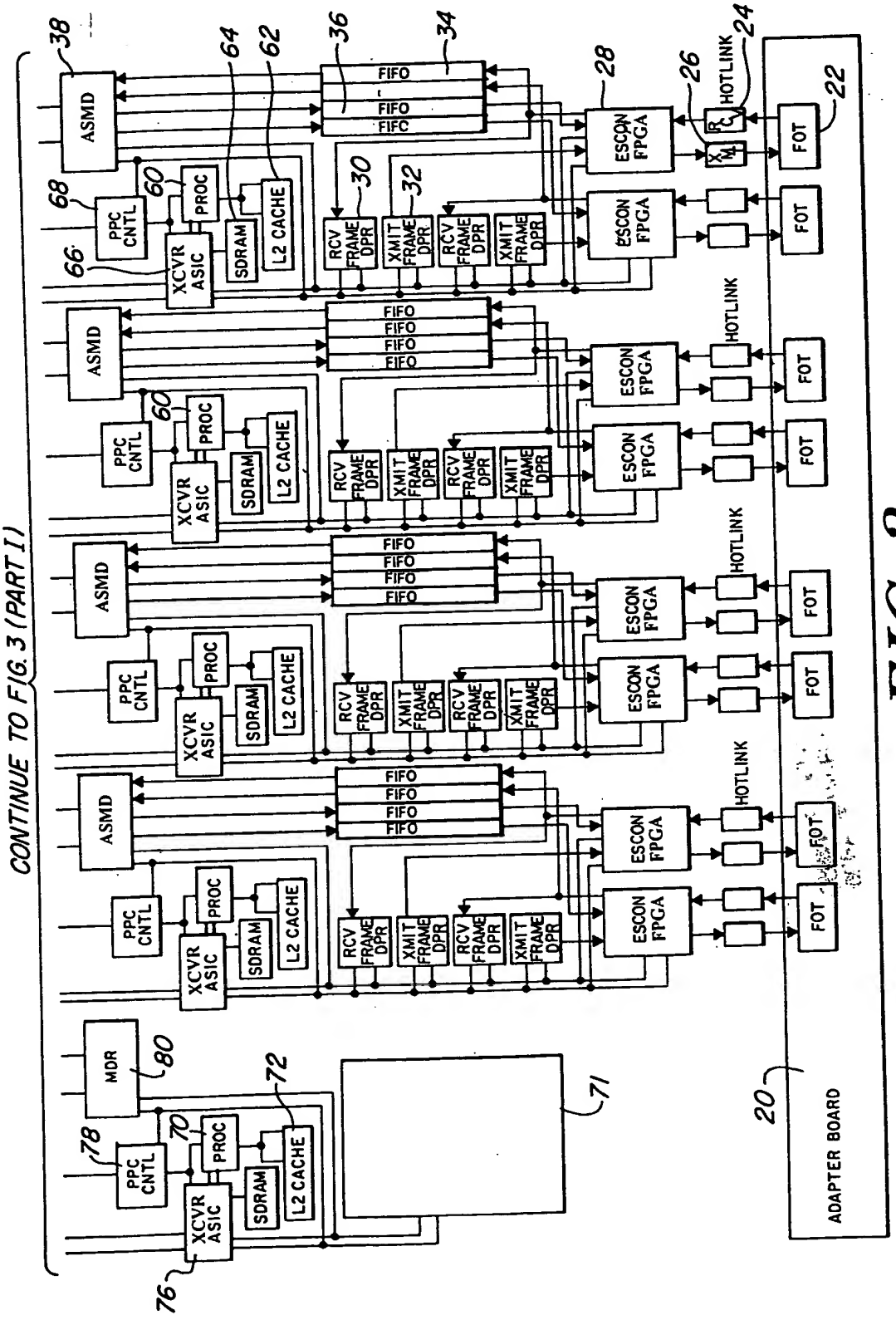

CONTINUE TO FIG. 3 (PART I)
ASMD
FIFO
ESCON FPGA
HOTLINK
FOT
PPC CNTL
PROC
SDRAM
L2 CACHE
XCVR ASIC
RCV FRAME DPR
XMIT FRAME DPR
MDR
ADAPTER BOARD
38
64
62
36
34
28
26
24
22
68
60
66
30
32
80
72
78
70
71
20
76

FIG. 3 (PART II)

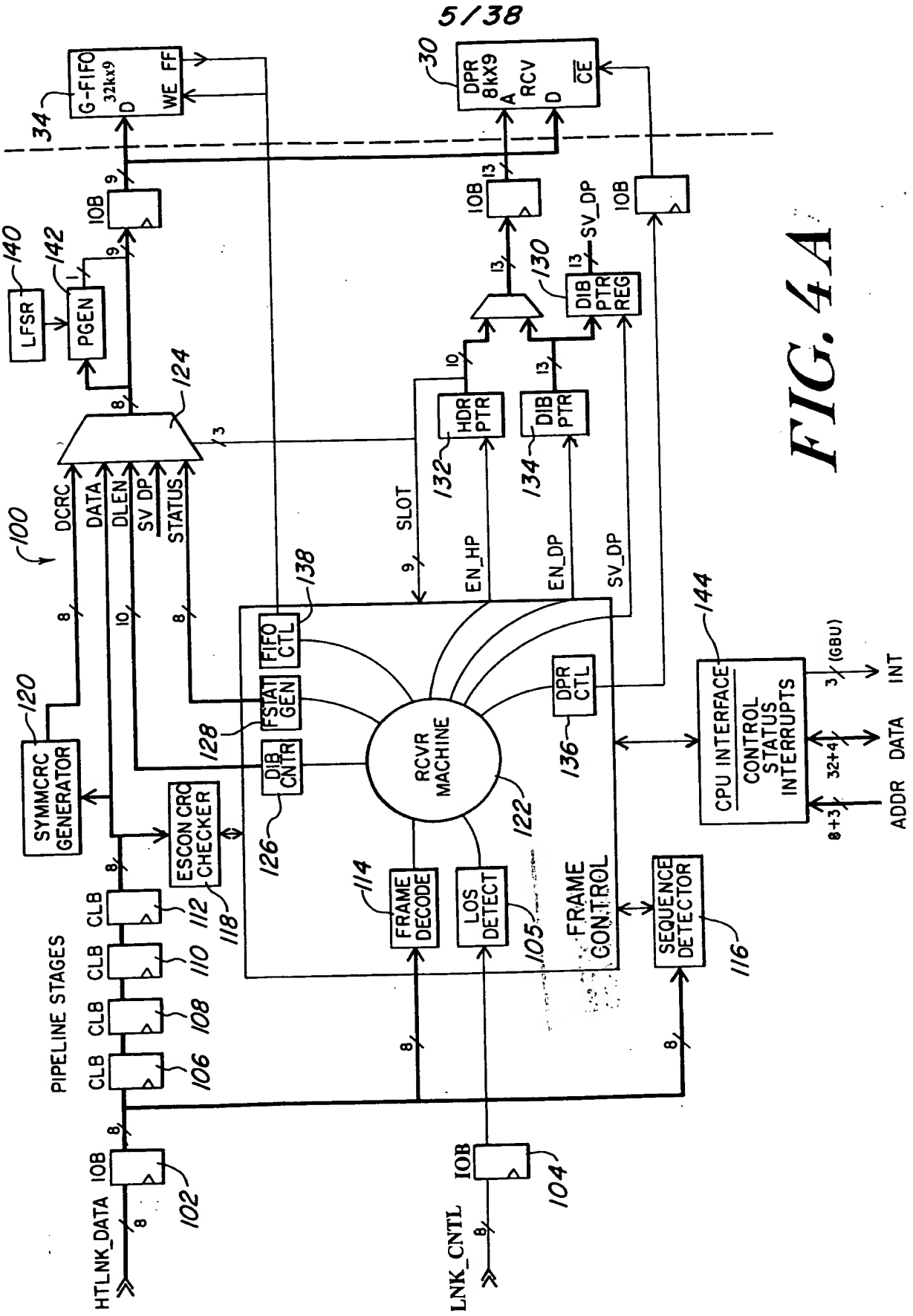
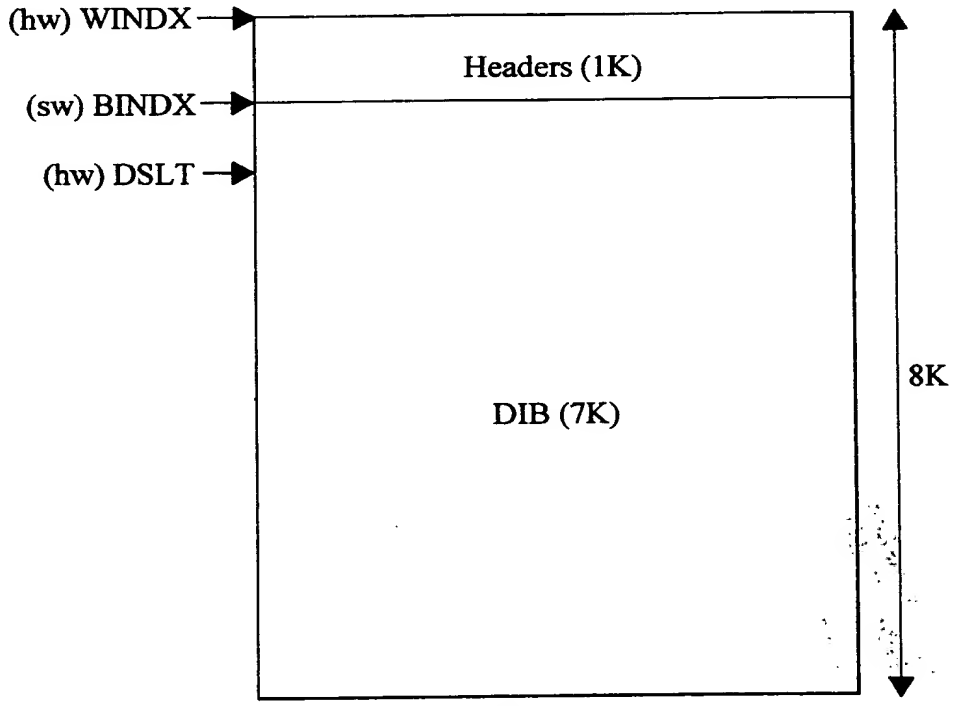

G-FIFO 32kx9
WE FF
D
34
DPR 8kX9
A RCV D CE
30
IOB
LFSR
PGEN
140
142
124
DCRC
DATA
DLEN
SV DP
STATUS
100
SLOT
HDR PTR
DIB PTR
132
134
130
DIB PTR REG
SV_DP
EN_HP
EN_DP
FIFO CTL
138
FSTAT GEN
DIB CNTR
128
126
SYMMCRC GENERATOR
120
ESCON CRC CHECKER
118
RCVR MACHINE
122
DPR CTL
136
144
CPU INTERFACE
CONTROL
STATUS
INTERRUPTS
(GBU)
INT
DATA
ADDR
32+4
8+3
FRAME DECODE
114
LOS DETECT
105
FRAME CONTROL
SEQUENCE DETECTOR
116
CLB
112
110
108
106
PIPELINE STAGES
HTLNK_DATA
102
LNK_CNTL
104

FIG. 4A



Receiver Frame Store

Allocation Map.

FIG. 4B

	0	7	8	15
0	Data Adr			DSLT
1	Data Len			
2	Fstatus		SCRC	
3	Dest Link Addr		0000	Dest Log Adr
4	Src Link Addr		0000	Src Log Adr
5	Link Control		IFI	
6	Device Adr 0		Device Adr 1	
7	DHF		XX	

Device Frame

Header Structure.

FIG. 4C

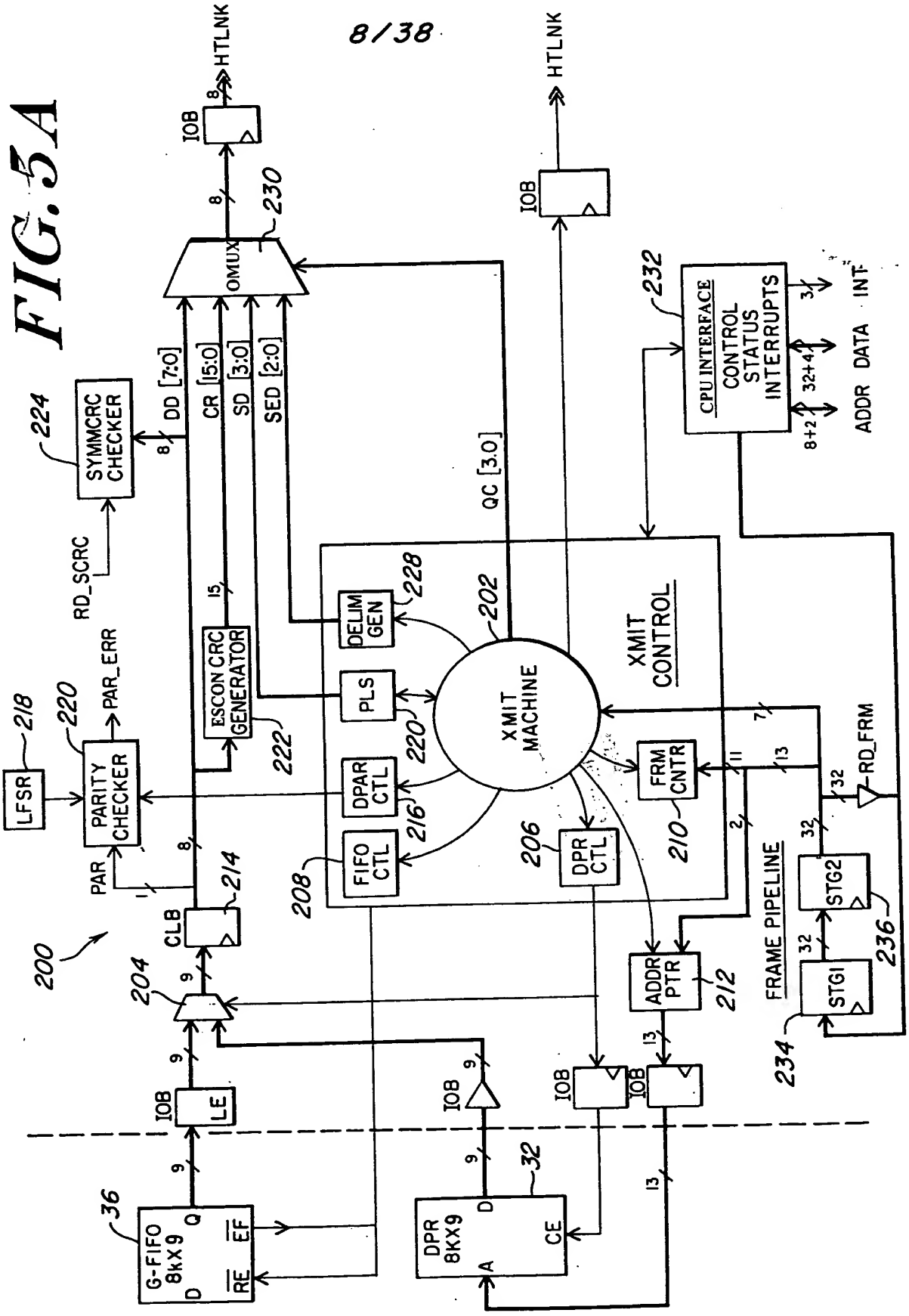
	0	7	8	15
0	Data Adr			DSLT
1	Data Len			
2	Fstatus		XX	
3	Dest Link Addr		0000	Dest Log Adr
4	Src Link Addr		0000	Src Log Adr
5	Link Control		XX	

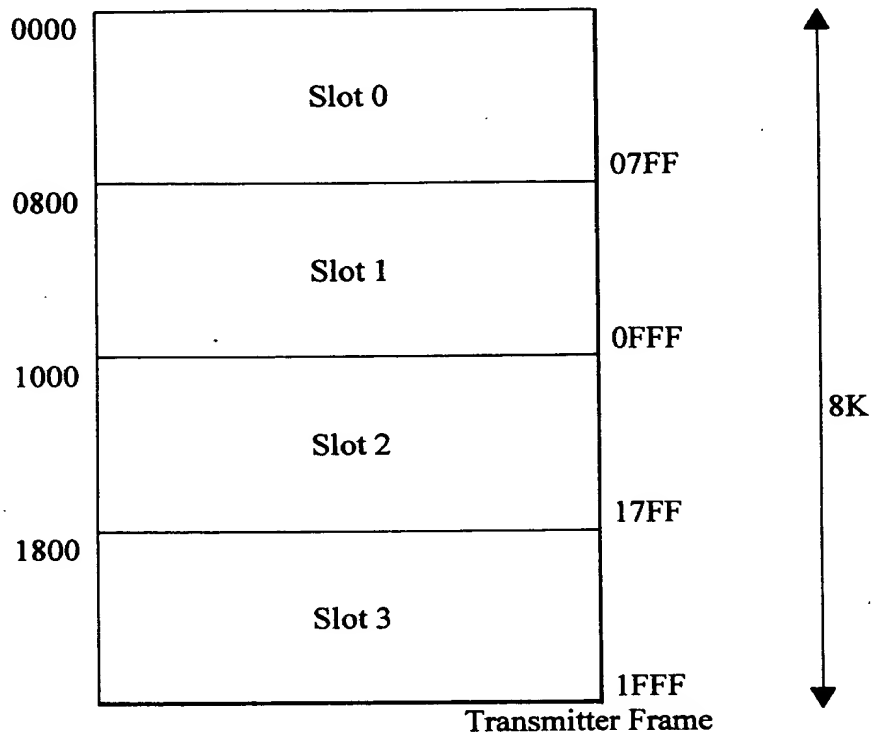
Link Frame Header

Structure.

FIG. 4D

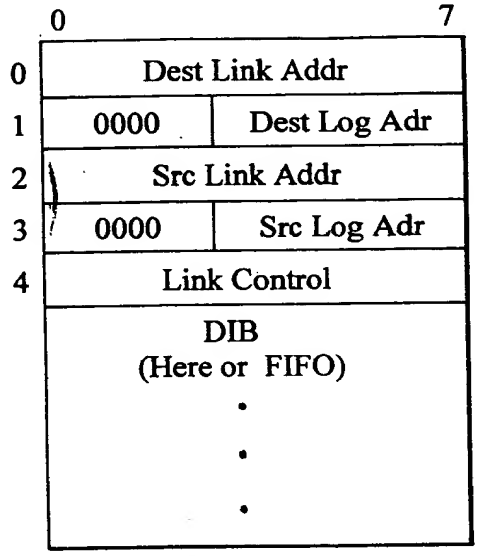
FIG. 5A


HTLNK
IOB
OMUX
230
SYMMCRC CHECKER
224
DD [7:0]
CR [15:0]
SD [3:0]
SED [2:0]
QC [3.0]
RD_SCRC
PAR_ERR
ESCON CRC GENERATOR
222
DELIM GEN
228
PLS
220
XMIT MACHINE
202
XMIT CONTROL
CPU INTERFACE
CONTROL
STATUS
INTERRUPTS
232
ADDR DATA INT
LFSR
218
PARITY CHECKER
DPAR CTL
216
FIFO CTL
208
DPR CTL
206
FRM CNTR
210
RD_FRM
PAR
CLB
214
200
204
ADDR PTR
212
FRAME PIPELINE
STG2
STG1
236
234
LE
G-FIFO 8kX9
36
DPR 8KX9
32



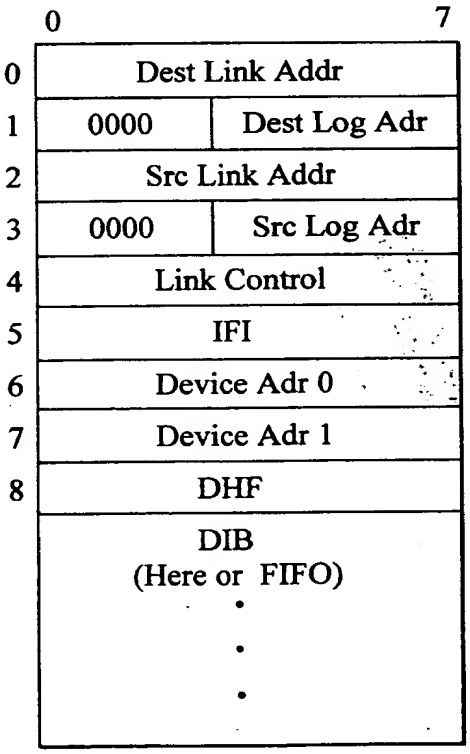
Store Allocation Map.

FIG. 5B



Link Frame Header Structure.

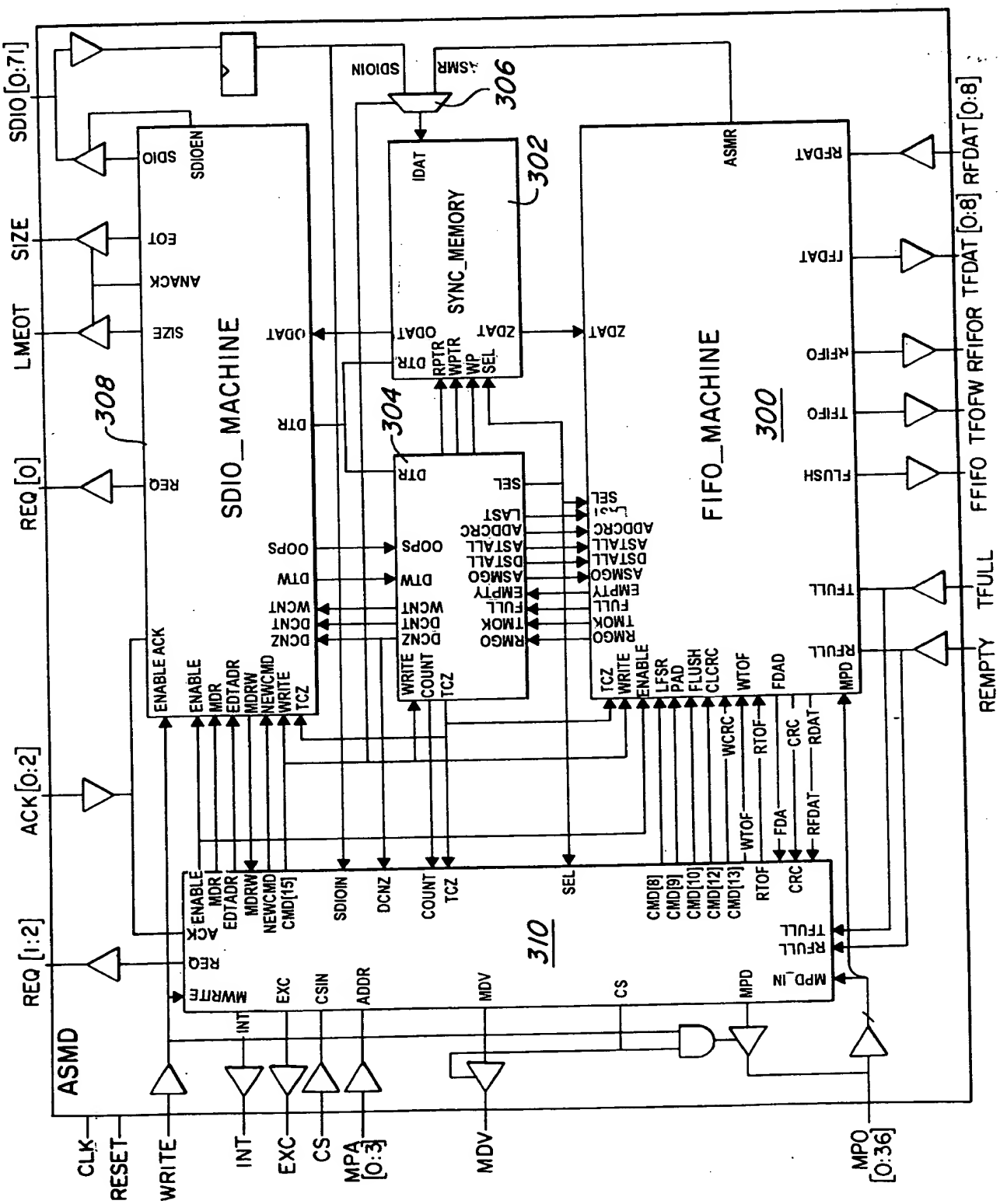
FIG. 5C



Device Frame Header Structure

FIG. 5D

FIG. 6


38
SDIO[0:7]
SIZE
LMEOT
REQ[0]
ACK[0:2]
REQ[1:2]
SDIO_MACHINE
308
SDIO
SDIOEN
EOT
ANACK
SIZE
REQ
ODAT
DTR
SDIOIN
ASMR
306
SYNC_MEMORY
302
IDAT
ODAT
ZDAT
DTR
RPTR
WPTR
WP
SEL
304
FIFO_MACHINE
300
ASMR
RFDAT
TFDAT[0:8]
RFDAT[0:8]
RFIFO
TFIFO
FLUSH
TFULL
RFULL
FFIFO
TFOFW
RFIFOR
TFULL
REMPTY
ENABLE ACK
ENABLE
MDR
EDTADR
MDRW
NEWCMD
WRITE
TCZ
OOPS
DTW
WCNT
DCNZ
WRITE
COUNT
TCZ
SEL
LAST
ADDCRC
ASTALL
DSTALL
ASMGO
EMPTY
FULL
TMOK
RMGO
TCZ
WRITE
ENABLE
LFSR
PAD
FLUSH
CLCRC
WTOF
FDAD
MPD
WCRC
RTOF
CRC
RDAT
FDA
ENABLE
MDR
EDTADR
MDRW
NEWCMD
CMD[15]
SDIOIN
DCNZ
COUNT
TCZ
SEL
CMD[8]
CMD[9]
CMD[10]
CMD[12]
CMD[13]
RTOF
CRC
WTOF
FDA
RFDAT
310
ACK
REQ
MWRITE
EXC
CSIN
ADDR
MDV
CS
MPD
MPD_IN
TFULL
RFULL
INT
ASMD
CLK
RESET
WRITE
INT
EXC
CS
MPA[0:3]
MDV
MPO[0:36]

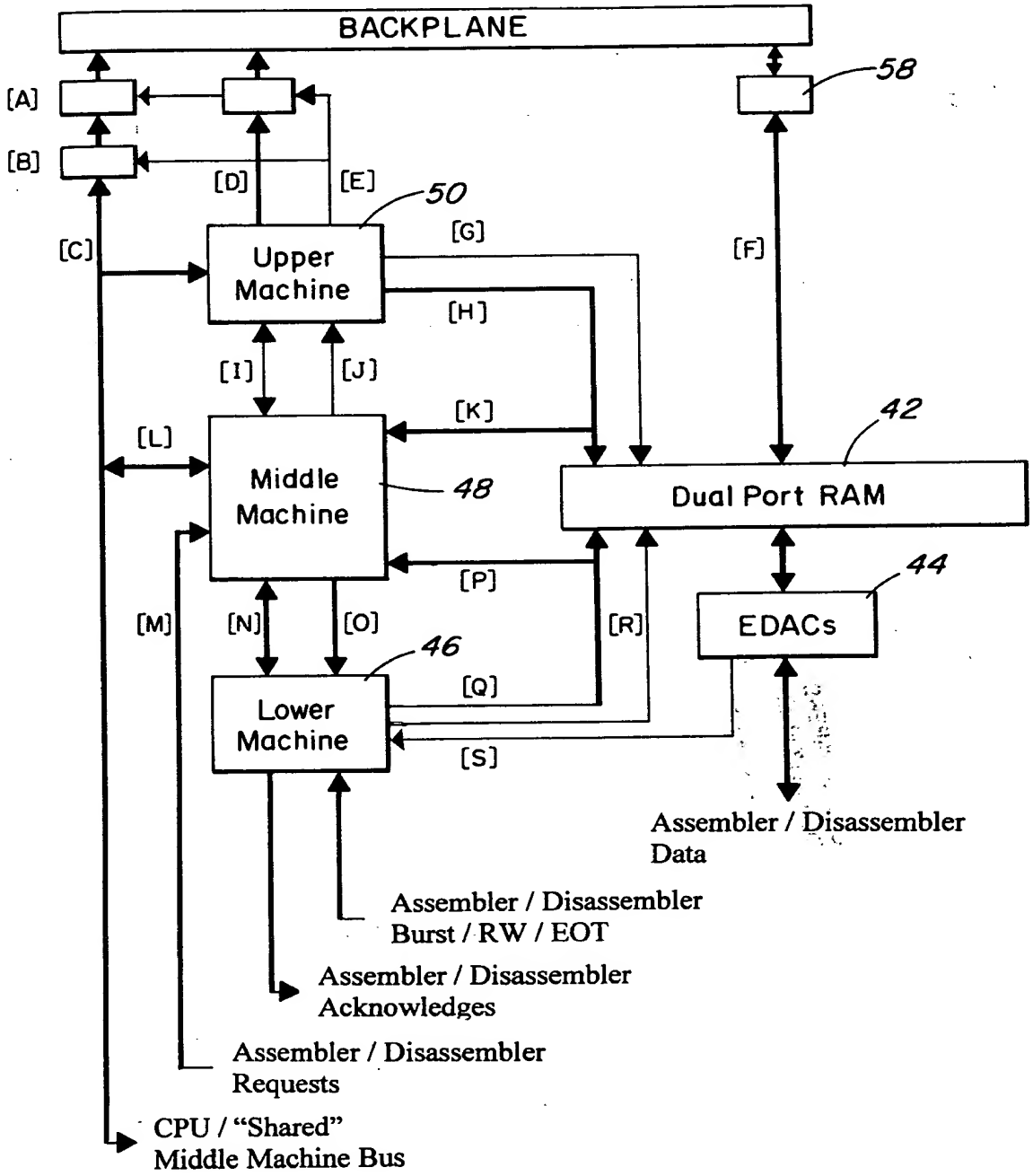
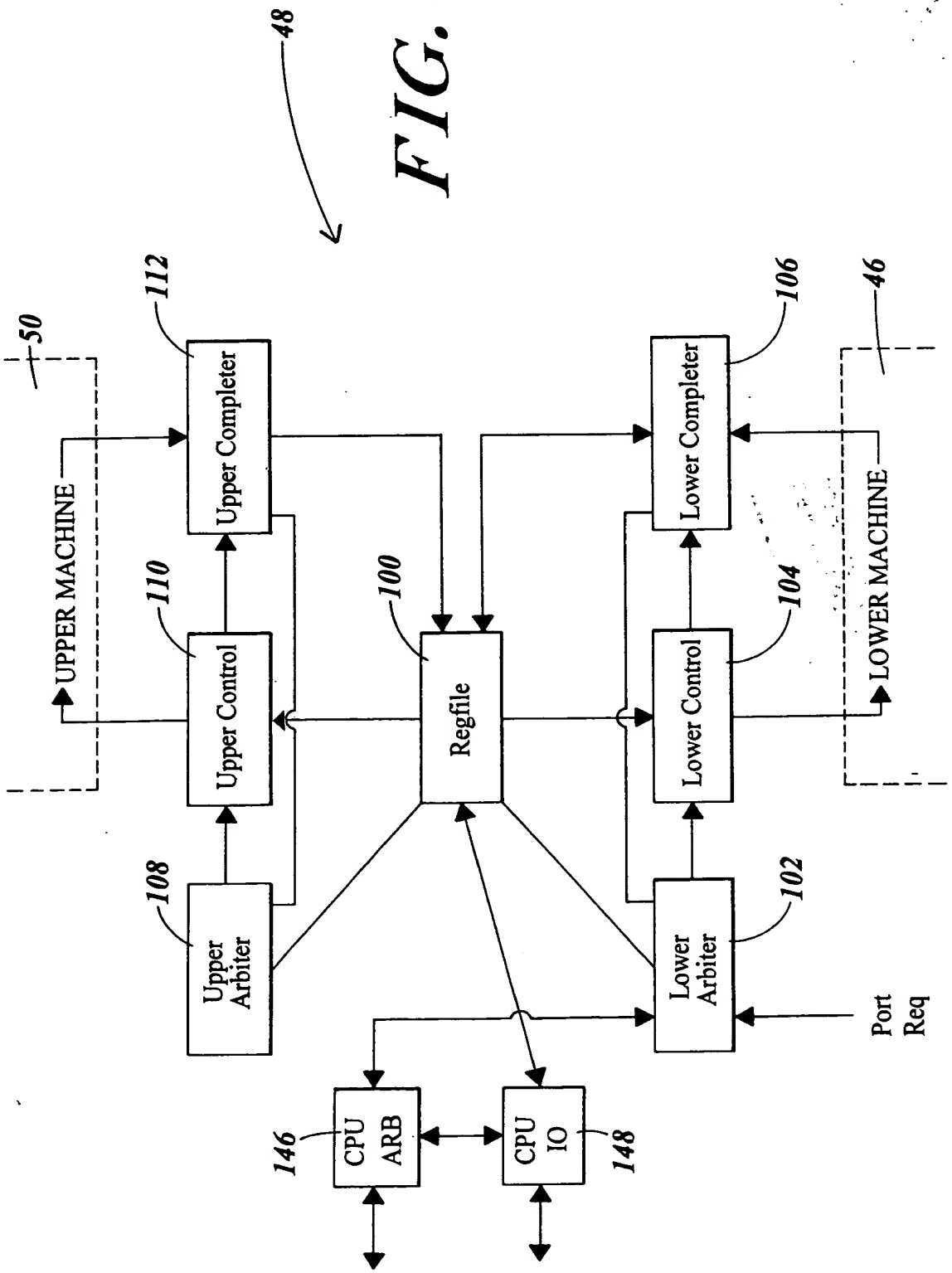

BACKPLANE
58
[A]
[B]
[C]
[D]
[E]
50
[G]
[F]
Upper Machine
[H]
[I]
[J]
[K]
42
[L]
Middle Machine
48
Dual Port RAM
[P]
44
[M]
[N]
[O]
[R]
EDACs
46
[Q]
Lower Machine
[S]
Assembler / Disassembler Data
Assembler / Disassembler Burst / RW / EOT
Assembler / Disassembler Acknowledges
Assembler / Disassembler Requests
CPU / "Shared" Middle Machine Bus

FIG. 7

FIG. 8


48
50
112
106
46
UPPER MACHINE
Upper Completer
Lower Completer
LOWER MACHINE
110
100
104
Upper Control
Regfile
Lower Control
108
102
Upper Arbiter
Lower Arbiter
Port Req
146
CPU ARB
CPU IO
148

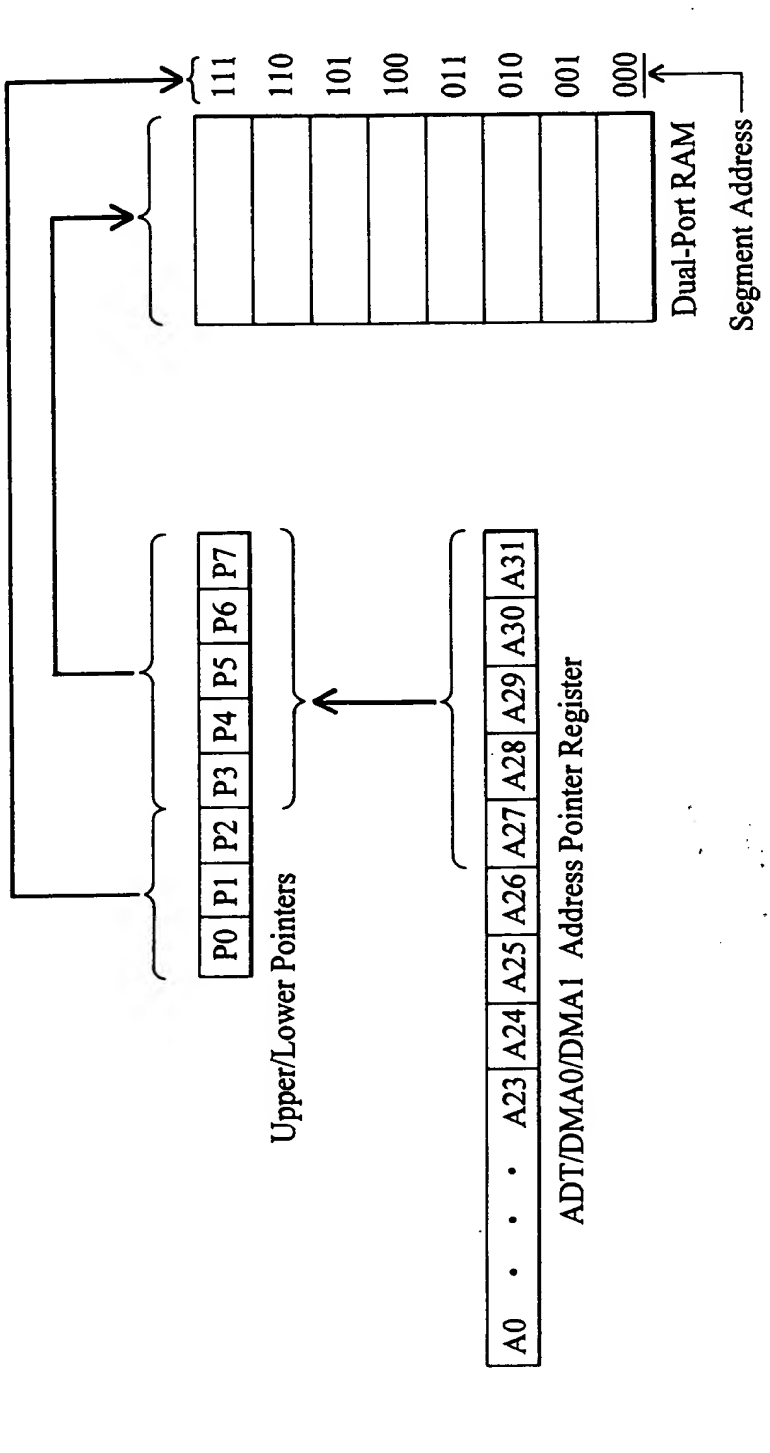
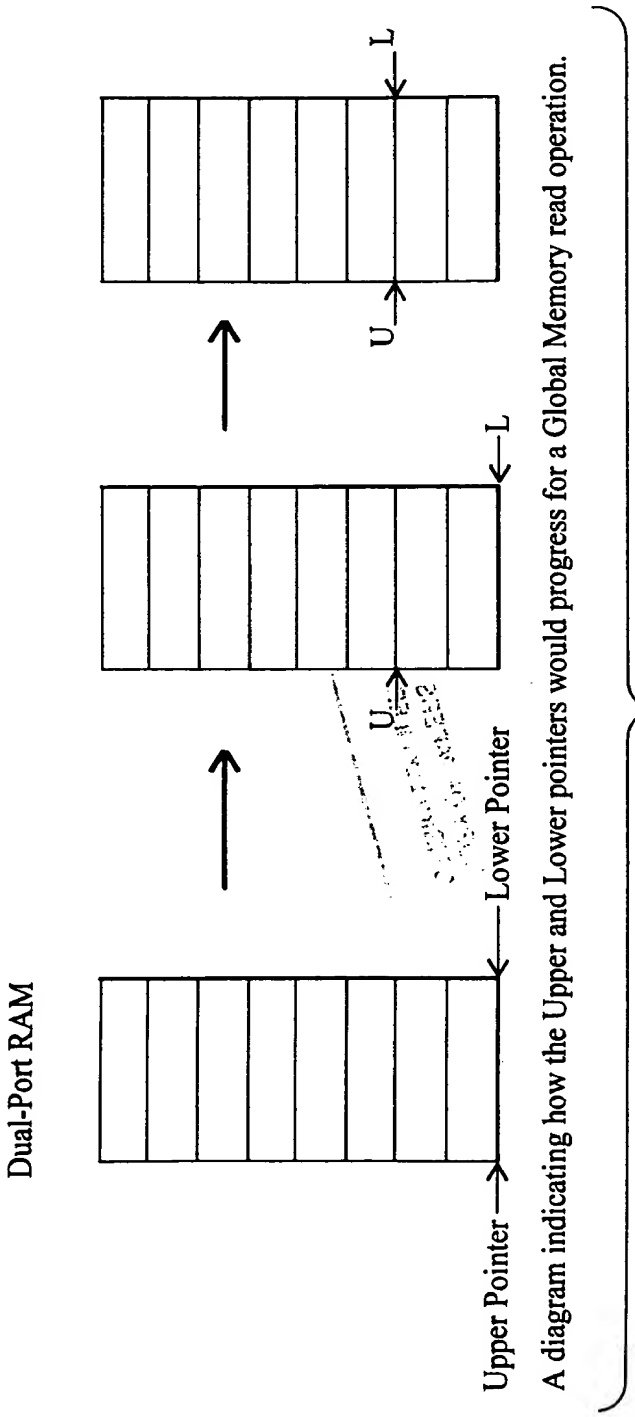


diagram shows the relationship between the Global Memory address and the Upper/Lower pointers

FIG. 9



A diagram indicating how the Upper and Lower pointers would progress for a Global Memory read operation.

FIG. 10

Lower Arbiter

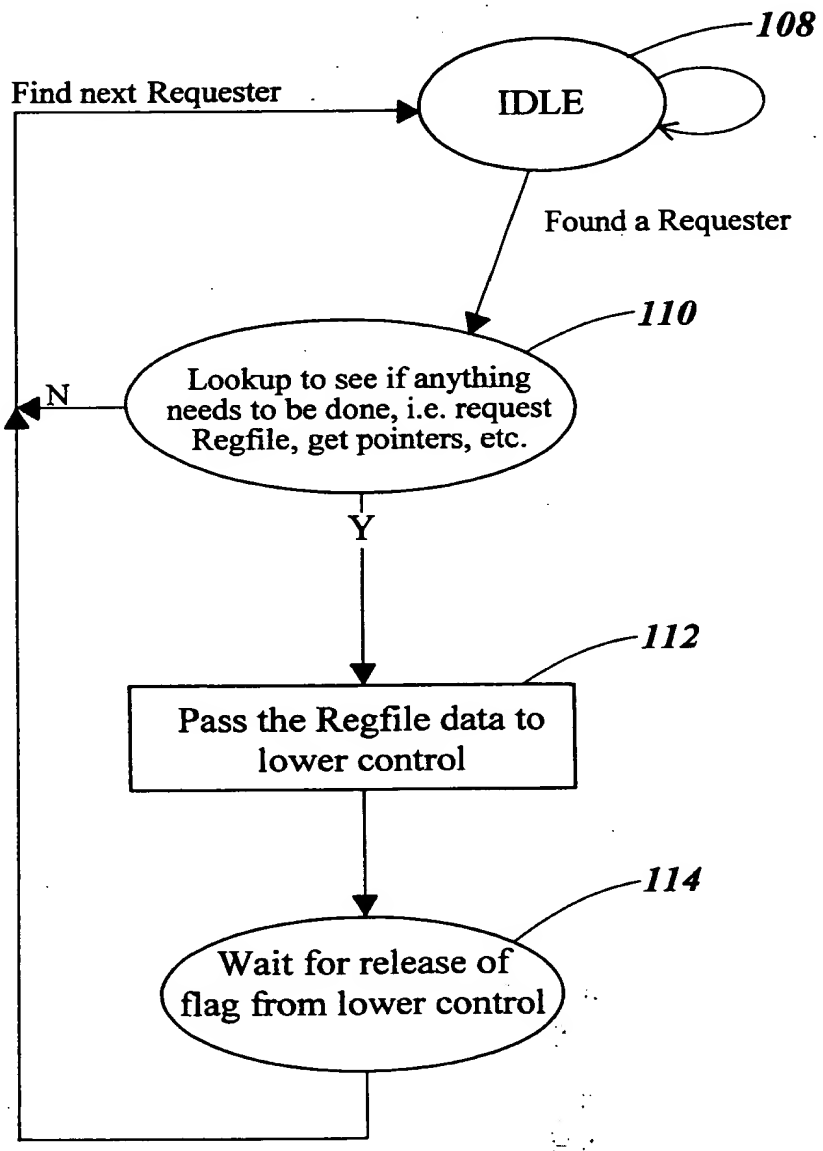


FIG. 11

Lower Control

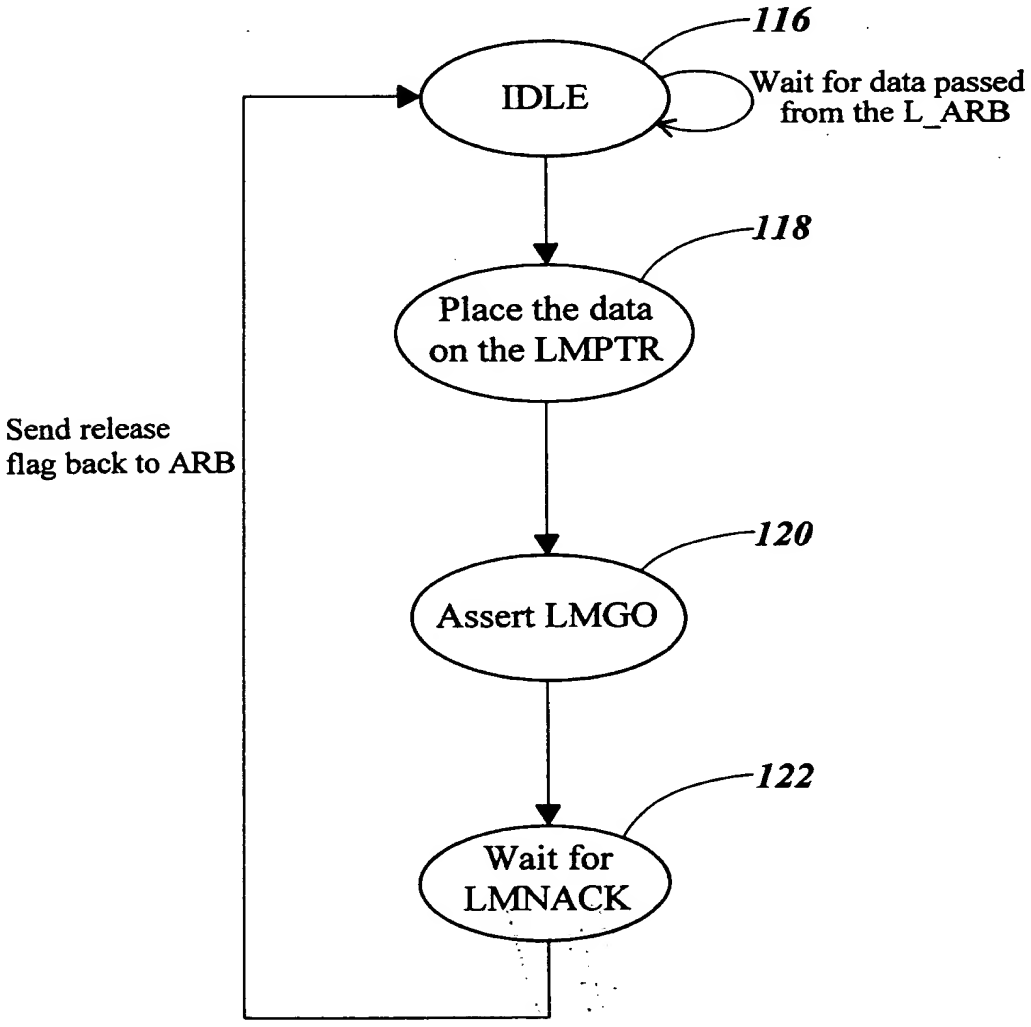


FIG. 12

Lower Completer

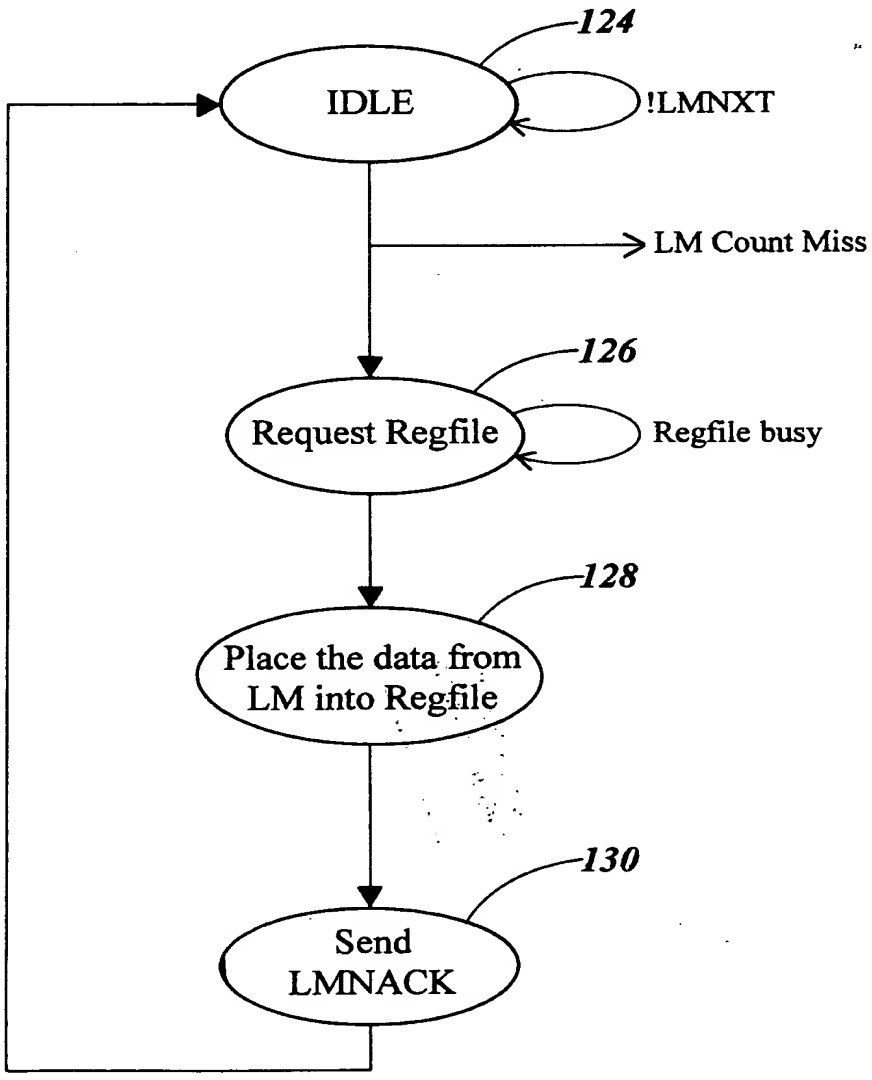


FIG. 13

Upper Arbiter

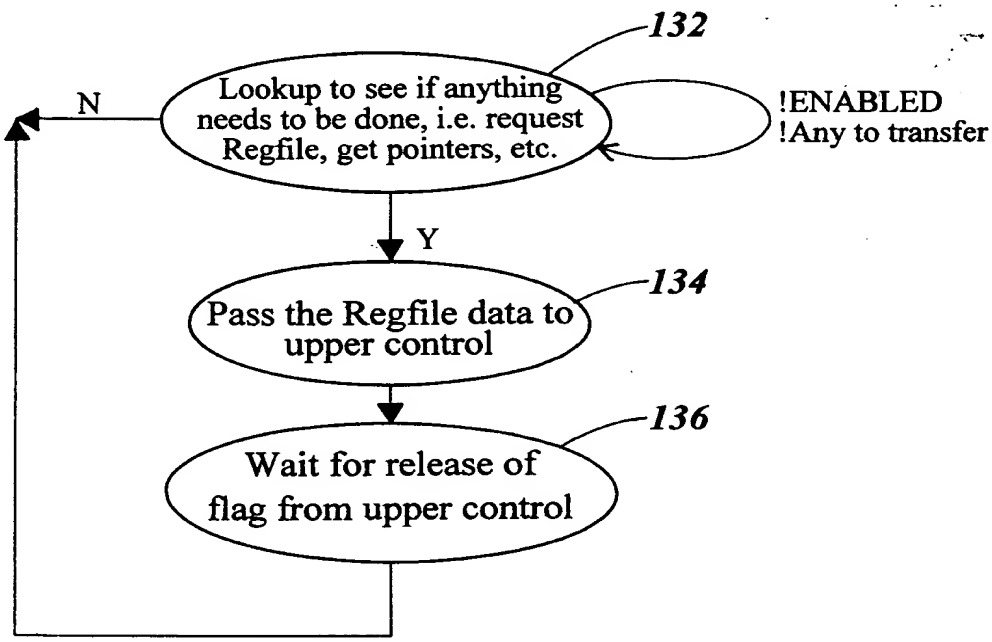


FIG. 14

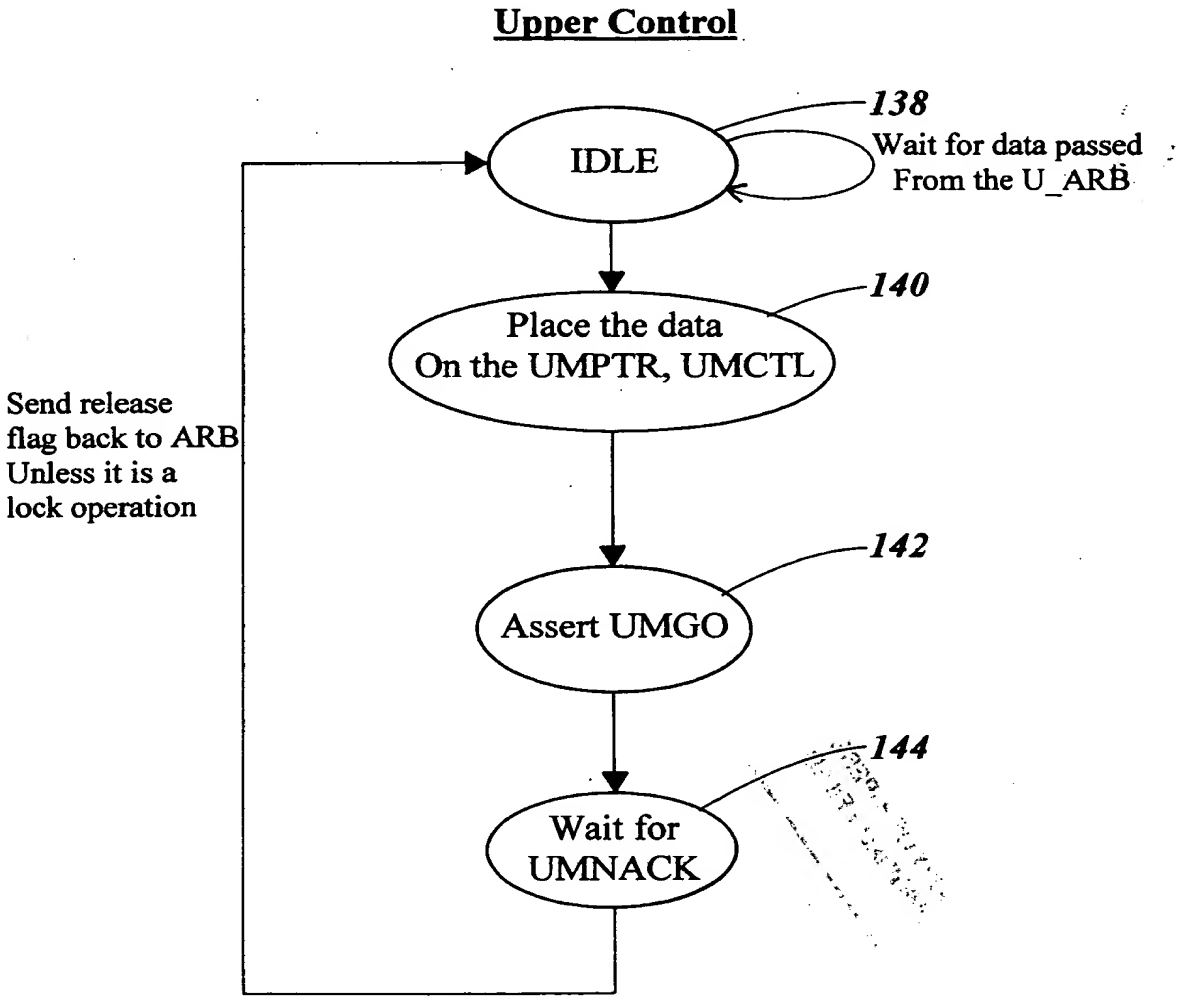

Upper Control
138
IDLE
Wait for data passed
From the U_ARB
140
Place the data
On the UMPTR, UMCTL
Send release
flag back to ARB
Unless it is a
lock operation
142
Assert UMGO
144
Wait for
UMNACK

FIG. 15

UPPER COMPLETER

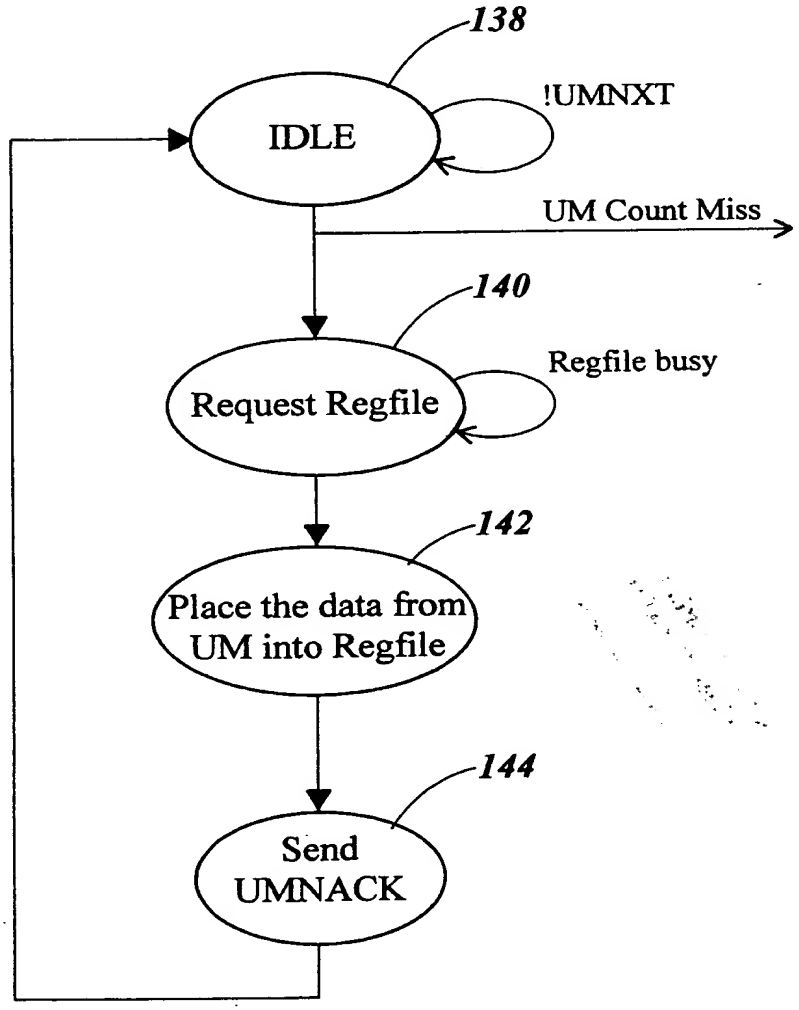


FIG. 16

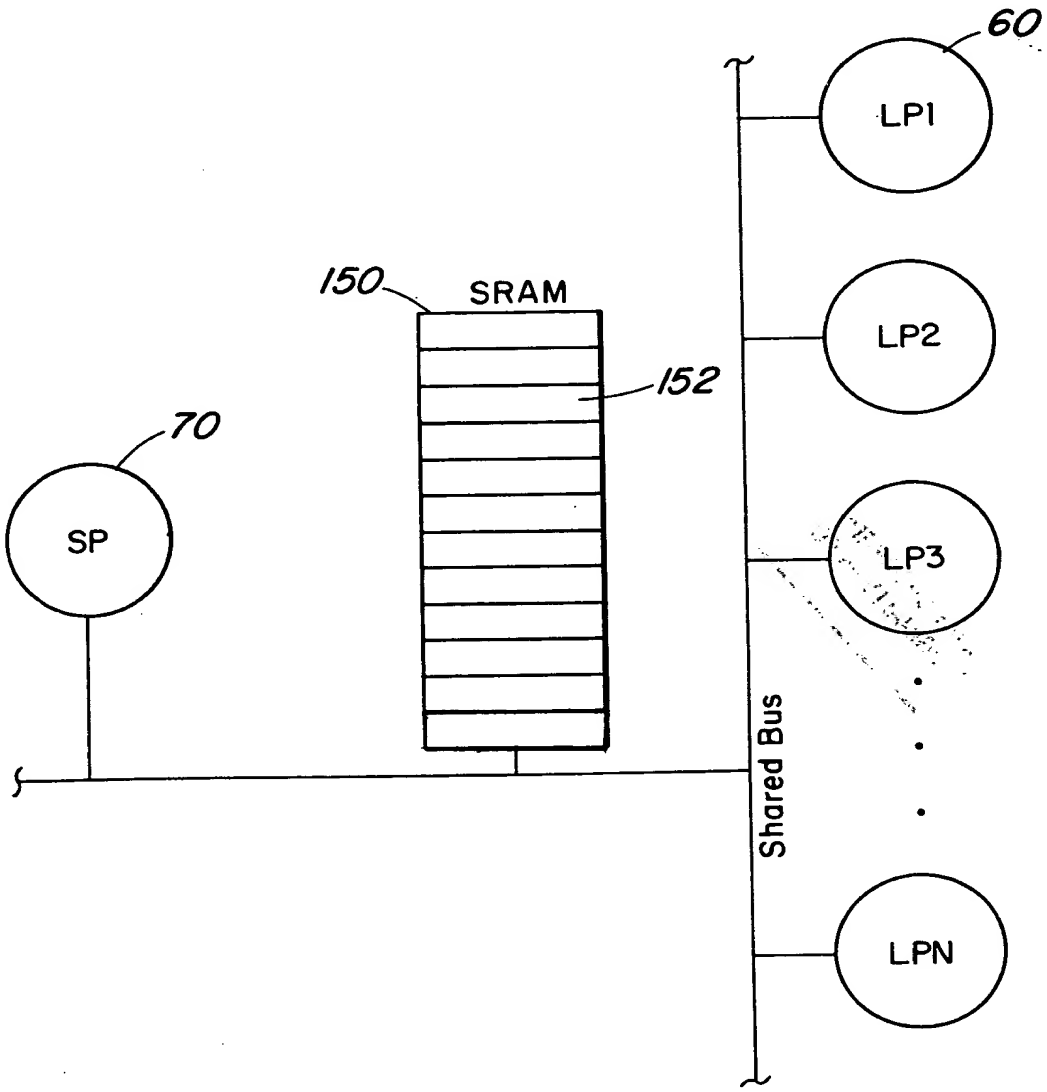


FIG. 17

Table I

Mnemonic	Size	Description
Data Adr	16b	FrameStore Location of data (DIB) portion of frame. If Data Addr=0x0000, DIB is in G-FIFO.
DSLT	3b	DSLT is actually the 3 low-order bits of Data Addr. If DSLT=0x0, the DIB is in G-FIFO. If DSLT=0x1 thru 0x7, the DIB is in the corresponding FrameStore slot.
Data Len	11b	Length of data (DIB) portion of frame. Does not include frame header or Escon CRC.
Fstatus	8b	0 3 4 5 6 7 ERROR | Full | 0 | EOF | SOF **ERROR:** 0000 = No Error 0001 = CRC Error 0010 = Control character received in frame 0011 = Invalid character received in frame 0100 = Maximum size of frame exceeded 0101 = Frame reception ended by 2 IDLE characters 0110 = Frame reception ended by ABORT delimiter 0111 = Frame reception ended by Invalid EOF delimiter *The following errors cause Frame Reception to stop* 1000 = Frame reception ended by LOS detection 1001 = Frame reception ended by Sequence detection 1010 = Frame reception by SOF delimiter 1100 = Frame reception ended by G-FIFO overflow Full: 1=This frame caused the FrameStore header section to become Full. EOF: 0=PEOF detected; 1=DEOF detected SOF: 0=PSOF detected; 1=CSOF detected
SCRC	8b	CRC covering DIB of received frame. Only valid for Device-frames independent of Whether the DIB goes to FrameStore or G-FIFO.

FIG. 18

Applicants: Reena Gupta, Yao Wang, and Alesia Tringale
U.S.S.N.: 09/213,613 / Confirm. No. 6656
Title: *Messaging Mechanism for Inter Processor Communic*
Filing Date: December 18, 1998 / Docket No.: EMC-97-060
Attorney: Krishnendu Gupta, Esq. (Reg. No. 37,977)

Table II

8100 0320 [WO] : ESCON Receiver Control Register

0				4				8				12				16				20				24			28				
CMC	RSVD	RSVD	FSt	CBER	RSVD	RSVD	RSVD	EnG	G	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	EnBx	RSVD	RSVD	BINDX	BINDX	BINDX	BINDX	BINDX
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W

Mnemonic	Size	Description	Notes
CMC	1b	1=Clear Machine Check conditions	
FSt	1b	1=Enable Frame Reception (Clear STOPPED Interrupt and conditions)	
CBER	1b	1=Clear BER Condition	
EnG	1b	1=Enable loading G bit	
G	1b	1=Put next incoming frame into G-FIFO 0=Put next incoming frame into FrameStore	
EnBx	1b	1=Enable loading BINDX	
BINDX	5b	Boundary Index (written only when EnBx = 1)	

FIG. 19

Table III

8100 0320 [RO] : ESCON Receiver Status Register

0				4				8				12				16		20				24				28					
DPE	SQI	FRI	STP	GF	FOVF	GOVF	ABN	FULL	G	BSY	FRM	SEQ	SEQ	SEQ	SEQ	SEQ	LOS	RSVD	RSVD	RSVD	WINDX	WINDX	WINDX	WINDX	WINDX	RSVD	BINDX	BINDX	BINDX	BINDX	BINDX
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Mnemonic	Size	Description	Notes
DPE	1b	1=CPU Data Parity Error on Write (Cleared when RcvCtl/CMC is asserted	UGLY
SQI	1b	1=Sequence interrupt status (Cleared immediately after RcvStat register is read)	GOOD
FRI	1b	1=Frame interrupt status (Cleared immediately after RcvStat register is read)	GOOD
STP	1b	1=Stopped interrupt status	BAD
GF	1b	1=Receiver G-FIFO Full. This bit is "live" status of the 'Full' flag.	
FOVF	1b	1=Overflow condition detected on FrameStore (causes STP to assert)	BAD
GOVF	1b	1=Overflow condition detected on G-FIFO (causes STP to assert)	BAD
ABN	1b	1=Abnormal condition detected (causes STP to assert)	BAD
FULL	1b	1=FrameStore full. No more frames allowed in FrameStore or G-FIFO because header section of FrameStore is full as defined by BINDX (Cleared on writing RcvCtl/BINDX)	
G	1b	G-bit status	
BSY	1b	1=Receiver Framestore Busy Error	BAD
FRM	1b	1=Frame was received	GOOD
SEQ	5b	Sequence being received on the link: 1xxxx : Rsvd_Seq x1xxx : IDLE 00100 : NOS 00101 : UD 00110 : UDR 00111 : OFL	GOOD (Cleared immediately after RcvStat register is read)
LOS	1b	1=LossOfSync (LOS) Detected	
WINDX	5b	Slot number for NEXT received frame	
BINDX	5b	Current Boundary Slot number	

FIG. 20

Applicants: Reema Gupta, Yao Wang, and Alesia Tringale
U.S.S.N.: 09/213,613 / Confirm. No. 6656
Title: *Messaging Mechanism for Inter Processor Communication*
Filing Date: December 18, 1998 / Docket No.: EMC-97-060
Attorney: Krishnendu Gupta, Esq. (Reg. No. 37,977)

Table IV

8100 0324 [RW] : ESCON Receiver Mask-Miscellaneous Register

0						4						8				12				16				20				24				28			
StpEn	LoSEn	RsqEn	IdlEn	VsqEn	FrmEn	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	HLB	EnDisp	Busy	BER	RSVD	RSVD	RSVD	RSVD	MajR	MajR	MajR	MajR	MinR	MinR	MinR	MinR
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RW	RW	RW	RW	RW	RW	R	R	R	R	R	R	R	R	R	R	RW	RW	RW	RW	R	R	R	R	R	R	R	R	R	R	R	R

Mnemonic	Size	Description	Notes
StpEn	1b	1=Enable Stop Interrupt	
LoSEn	1b	1=Enable LOS Interrupt	
RsqEn	1b	1=Enable Rsq interrupt	
IdlEn	1b	1=Enable Idle interrupt	
VsqEn	1b	1=Enable VSQ interrupt	
FrmEn	1b	1=Enable Frame interrupt	
HLB	1b	Enable Hotlink Loopback: 1=Receive data from Hotlink Transmitter 0=Receive data from Optical Link	
EnDisp	1b	1=Enable G-FIFO disparity generator	
Busy	1b	1=Software is busy. Instruct hardware to return Link-Busy for connection frames.	
BER	1b	1=Bit-error Violation detected.	Software must write '1' to clear this bit.
MajR	4b	Major Revision of RCVR LCA	Read-Only
MinR	4b	Minor Revision of RCVR LCA	Read-Only

FIG. 21

Applicants: Reema Gupta, Yao Wang, and Alesia Tringale
U.S.S.N.: 09/213,613 / Confirm. No. 6656
Title: *Messaging Mechanism for Inter Processor Communi*
Filing Date: December 18, 1998 / Docket No.: EMC-97-060
Attorney: Krishnendu Gupta, Esq. (Reg. No. 37,977)

Table V

8100 0328 [RW] : ESCON Receive Diagnostic Register

0				4				8				12				16				20			24					28			
RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	WrBOF	BOFD	BOFD	BOFD	BOFD	BOFD	BOFD	BOFD	BOFD
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	W	RW	RW	RW	RW	RW	RW	RW	RW

Mnemonic	Size	Description	Notes
WrBOF	1b	1=Execute write operation to incoming G-FIFO	Write-Only
BOFD	8b	Data byte to be written to incoming G-FIFO. Initializes to 00h when RCVR is reset.	

FIG. 22

Table VI

8100 0340 [RW] : ESCON Transmitter Frame Register

0							4						8						12						16						20						24						28				
TxSt	G	HLOC	HLOC	DELIM	DELIM	EnP	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	FrLen	FrLen	FrLen	FrLen	FrLen	FrLen	FrLen	FrLen	FrLen	FrLen	FrLen	FrLen										
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0										
W	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW										

Mnemonic	Size	Description	Notes
TxSt	1b	1=Start frame transmission	Write-Only
G	1b	Location of Frame DIB: 0=DIB in Frame Store 1=DIB in G-FIFO	Link frames should have bit clear; Device frames can have either clear/set
HLOC	2b	Location of Frame Header	
DELIM	2b	Frame Delimiters: 00=PSOF,PEOF 01=CSOF,PEOF 10=PSOF,DEOF 11=Not Defined	
EnP	1b	1=Enable Pacing (pacing bytes are appended to end of this frame)	
FrLen	11b	Frame Length (Header + DIB)	

FIG. 23

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Table VII

8100 0344 [WO] : ESCON Transmitter Control Register

0				4				8				12				16				20				24				28			
CMC	RSVD	CFE	FSEn	FEEn	CCRC	FXP	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W

Mnemonic	Size	Description	Notes
CMC	1b	1=Clear Machine Check conditions	
CFE	1b	1=Clear Frame-Error interrupt and conditions	
FSEn	1b	1=Enable Frame-Sent interrupt	
FEEn	1b	1=Enable Frame-Error interrupt	
CCRC	1b	1=Clear the Xmit G-FIFO Symmetrix CRC	
FXP	1b	1=Flush the entire Xmit pipeline	

FIG. 24

Table VIII

8100 0344 [RO] : ESCON Transmitter Status Register

0				4				8				12			16					20							24				28			
DPE	FS	FE	FSEn	FEEn	GMT	OVF	GPE	FPE	IW	IRQ	XPF	XPE	GE	BSY	RSVD	GCRC	GCRC	GCRC	GCRC	GCRC	GCRC	GCRC	GCRC	MajR	MajR	MajR	MajR	MinR	MinR	MinR	MinR
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Mnemonic	Size	Description	Notes
DPE	1b	1=CPU Data Parity Error on White (Cleared when XmtCtl/CMC is asserted)	UGLY
FS	1b	Frame-Sent status	GOOD
FE	1b	Frame-Error status	BAD
FSEn	1b	1=Frame-Sent interrupt enabled	
FEEn	1b	1=Frame-Error interrupt enabled	
GMT	1b	1=Xmit G-FIFO Empty (while sending frame)	BAD
OVF	1b	1=Frame Overflow (Frame > 1035 bytes)	BAD
GPE	1b	1=Xmit G-FIFO Parity Error	BAD
FPE	1b	1=Xmit FrameStore Parity Error	BAD
IW	1b	1=Illegal Write	BAD
IRQ	1b	1=Illegal Request	BAD
XPF	1b	1=Xmit Pipe Full	
XPE	1b	1=Xmit Pipe Empty	
GE	1b	1=Xmit G-FIFO Empty	live status/empty flag
BSY	1b	1=Xmit Framestore Busy Error	BAD
GCRC	8b	Xmit G-FIFO Symmetrix CRC	
MajR	4b	Major Revision of XMIT LCA	
MinR	4b	Minor Revision of XMIT LCA	

FIG. 25

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Table IX

8100 0348 [RW] : ESCON Transmitter Pacing-Loop-Sequence Register

0				4				8				12				16				20				24				28			
SEQ	SEQ	SEQ	SEQ	SDO	TXEN	EnDisp	RSVD	Pace	Pace	Pace	Pace	Pace	Pace	Pace	Pace	BIST	SVS	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	BLC	BLC	BLC	BLC	BLC	BLC	BLC	BLC
0 RW	0 RW	0 RW	0 RW	0 RW	0 RW	0 RW	0 RW	0 RW	0 RW	0 RW	0 RW	0 RW	0 RW	0 RW	0 RW	0 RW	0 RW	0 RW	0 RW	0 RW	0 RW	0 RW	0 RW	0 RW	0 RW	0 RW	0 RW	0 RW	0 RW	0 RW	0 RW

Mnemonic	Size	Description	Notes
SEQ	4b	Sequence Identifier 1111 : Offline 1001 : Not Operational 1011 : UD 1101 : UDR xxx0 : Idle 0xx1 : Reserved	
SDO	1b	1=Enable Pseudo Frame condition	
TXEN	1b	0=Enable Fiber-Optic Transmitter	Active-Low
EnDisp	1b	1=Enable Xmit G-FIFO disparity checker	
Pace	8b	Pacing Count – 1's complement	
BIST	1b	0=Enable Hotlink Built-In Self-Test (diagnostic)	not yet implemented
SVS	1b	1=Send Violation Sequence (diagnostic)	not yet implemented
BLC	8b	BIST Loop Counter (diagnostic)	not yet implemented

FIG. 26

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Table X

8100 034C [RO] : ESCON Transmitter Bottom-Of-FIFO Register

0				4				8				12				16				20				24				28			
RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	BOFD	BOFD	BOFD	BOFD	BOFD	BOFD	BOFD	BOFD
0 R	0 R	0 R	0 R	0 R	0 R	0 R	0 R	0 R	0 R	0 R	0 R	0 R	0 R	0 R	0 R	0 R	0 R	0 R	0 R	0 R	0 R	0 R	0 R	0 R	0 R	0 R	0 R	0 R	0 R	0 R	0 R

Mnemonic	Size	Description	Notes
BOFD	8b	Data byte read from outgoing G-FIFO	Read-Only

FIG. 27

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Table XI

8100 0310 [RW]: Assembler / Disassembler Command Register

0					4							8							12							16							20							24							28
EnXfr	DIR	EnDSP	wCRC	FF	RSVD	RSVD	PAD	Acrc0	Acrc1	Acrc2	Acrc3	Acrc4	Acrc5	Acrc6	Acrc7	XCO	XC1	XC2	XC3	XC4	XC5	XC6	XC7	XC8	XC9	XC10	XC11	XC12	XC13	XC14	XC15																
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0																
RW	RW	RW	RW	RW	R	R	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW																

Mnemonic	Size	Description	Notes
EnXfr	1b	1=Enable Transfer	
Dir	1b	1=Write (line to DPR) 0=Read (DPR to Line)	
EnDSP	1b	1=Enable disparity generator	
wCRC	1b	1=Enable appending CRC to end of data	
FF	1b	1=Flush FIFO	
PAD	1b	1=Enable 0 padding through ADT pipe	
Acrc0-Acrc7	8b	Accumulated CRC for current transfer	
XC0-XC15	16b	Number of bytes to transfer	Readback gives # of bytes remaining to transfer

FIG. 28

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Table XII

8100 0314 [RW] : Assembler / Disassembler Status Register

0								4								8								12								16								20								24								28							
CC	Idle	REQ	CRCnz	RxFnE	TxFF	RSVD	PAD	XPErr	PDErr	PAErr	PRErr	RSVD	RSVD	RSVD	RSVD	MajR	MajR	MajR	MajR	MajR	MajR	MajR	MajR	MinR	MinR	MinR	MinR	MinR	MinR	MinR	MinR
0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
RW	R	R	R	R	R	R	RW	RW	RW	RW	RW	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Mnemonic	Size	Description	Notes
CC	1b	1=Machine is Idle	
REQ	1b	1=ADT Request Outstanding to Middle Machine	*H/W diagnostic use*
PFErr	1b	1=Parity Error in SCSI transfer	BAD
Pderr	1b	1=Processor Data Bus Parity Error detected	BAD
Paerr	1b	1=Processor Address Bus Parity Error Detected	BAD
CRCErr	1b	1=CRC not zero	
Acrc0-Acrc7	8b	Accumulated CRC for current transfer	
CC0-CC15	16b	Current transfer count	

FIG. 29

Table XIII

8100 0300 [RW]: ADT Primary Address Pointer
8100 0700 [RW]: DMA0 Primary Address Pointer
8100 0B00 [RW]: DMA1 Primary Address Pointer
8100 0F00 [RW]: COPY Primary Address Pointer

FIG. 30

0				4				8				12				16				20				24				28			
AD0	AD1	AD2	AD3	AD4	AD5	AD6	AD7	AD8	AD9	AD10	AD11	AD12	AD13	AD14	AD15	AD16	AD17	AD18	AD19	AD20	AD21	AD22	AD23	AD24	AD25	AD26	AD27	AD28	AD29	AD30	AD31
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Mnemonic	Size	Description	Notes
AD0-AD31	32b	Primary Global Memory Dword Address, or Source Address for COPY operation	

Table XIV

8100 0304 [RW] : ADT Mirror / Copy Address Pointer
8100 0704 [RW] : DMA0 Mirror / Copy Address Pointer
8100 0B04 [RW] : DMA1 Mirror / Copy Address Pointer
8100 0F04 [RW] : COPY Mirror / Copy Address Pointer

FIG. 31

0				4				8				12				16				20				24				28			
AD0	AD1	AD2	AD3	AD4	AD5	AD6	AD7	AD8	AD9	AD10	AD11	AD12	AD13	AD14	AD15	AD16	AD17	AD18	AD19	AD20	AD21	AD22	AD23	AD24	AD25	AD26	AD27	AD28	AD29	AD30	AD31
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Mnemonic	Size	Description	Notes
AD0-AD31	32b	Mirror Global Memory Dword Address for Mirror Write Operations, or Destination Address for COPY operation	

Table XV

FIG. 32

8100 0308 [RW]: ADT Command & Transfer Length Register
8100 0708 [RW]: DMA0 Command & Transfer Length Register
8100 0B08 [RW]: DMA1 Command & Transfer Length Register
8100 0F08 [RW]: COPY Command & Transfer Length Register

0		4		8		12		16		20		24		28	
RSVD	RSVD	TL0	TL1	TL2	TL3	TL4	TL5	TL6	TL7	TL8	TL9	TL10	TL11	TL12	TL13
0 RW	0 RW	0 RW	0 RW	0 RW	0 RW	0 RW	0 RW	0 RW	0 RW	0 RW	0 RW	0 RW	0 RW	0 RW	0 RW
RSVD	RSVD	MIR	COPY	FP	IEC	FE	EOT	RSVD	RW	XOR	SVC	LOCK	RSVD	SPAR	EC
0 RW	0 RW	0 RW	0 RW	0 RW	0 RW	0 RW	0 RW	0 RW	0 RW	0 RW	0 RW	0 RW	0 RW	0 RW	0 RW

Mnemonic	Size	Description	Notes
TL0-TL13	14b	Number of Dwords to read or write	
MIR	1b	1=Mirror all Global Memory writes to the Mirror Address given in the Mirror Address Pointer	
COPY	1b	1=Perform a true DMA operation; Reads occur from the Primary Address Pointer, Writes are destined for the Copy Address Pointer; Transfer length is given by TL0-13.	RW must be set; SVC&MIR are illegal; XOR may be used
FP	1b	Middle Machine First Pass internal arbiter bit	Must be set to '1'
IEC	1b	Middle Machine Internal Enable Channel	Must be set to '1'
FE	1b	1=Fatal Error Occurred During Transfer	
EOT	1b	1=End Of Transfer has occurred 1=Force End Of Transfer protocol in Middle Machine	When Read When Written
RW	1b	1=Read 0=Write	
XOR	1b	1=XOR the new data with the current data in Global Memory, then store the result in Global Memory	Only valid for Writes with or without Mirror
SVC	1b	1=Backplane cycles will be initiated as Service Cycles	
LOCK	1b	1=Lock Memory	
RSVD	1b	Reserved Command bit	Mustbe set to '0'
SPAR	1b	Backplane SPARE bit	Must be set to '0'
EC	1b	1=Enable Channel 0=Disable Channel	An interrupt will be generated after the Middle Machine completes current pass

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Table XVI

8100 030C [RW]: ADT Status/Upper & Lower Pointers

8100 070C [RW]: DMA0 Status/Upper & Lower Pointers

8100 0B0C [RW]: DMA1 Status/Upper & Lower Pointers

8100 0F0C [RW]: COPY Status/Upper & Lower Pointers

0						4						8						12						16						20						24						28			
ERR	CTMS	ETNZ	UEC0	UEC1	MPE	RSVD	INITS	CCO	CC1	CC2	CC3	LECO	LEC1	LEC2	DMC	UPO	UP1	UP2	UP3	UP4	UP5	UP6	UP7	LPO	LP1	LP2	LP3	LP4	LP5	LP6	LP7													
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0													
RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW													

FIG. 33
PART I

Table XVI

Mnemonic	Size	Description	Notes
ERR	1b	1=An Error Occurred during the transfer	
CTMS	1b	1=Count Miss occurred	
ETNZ	1b	1=Ending Transfer Count Not Zero error occurred	
UECO-1	2b	Upper Error Codes	See table below
MPE	1b	1=Machine Parity Error occurred (CPU Parity Error / Internal Parity Error)	
INITS	1b	1=Global Memory reported Initial Status	
CC0-CC3	4b	Ending Global Memory Condition Codes	0101=good status
LEC0-2	3b	Lower Error Codes	See table below
DMC	1b	1=DMA Operation Completed	
UP0-UP7	8b	Upper Machine DPR Pointer	
LP0-LP7	8b	Lower Machine DPR Pointer	

M0/M1 Condition Codes:

Condition Code	Meaning	Notes
0101 (5)	Good Ending Status (No Errors)	
1001 (9)	Protocol Error	
1110 (E)	Count Miss	
1000 (8)	R/W Mismatch	
1010 (A)	Multi-bit Error	
0011 (3)	Single-bit Error	
0111 (7)	Memory Internal Error	
1101 (D)	More Than One Ending Status Error	

Upper Error Codes:

Code	Meaning
00 (0)	No Upper Machine Hardware Errors
01 (1)	Short Timeout Occurred
10 (2)	Long Timeout Occurred
11 (3)	Lock Timeout or Upper Machine Command Parity Error Occurred

Lower Error Codes:

Code	Meaning
000 (0)	No Lower Machine Hardware Errors
001 (1)	Single-Bit ECAC Error Detected
010 (2)	Reserved
011 (3)	Multi-Bit EDAC Error Detected
100 (4)	Parity Error detected on SDIO bus
101 (5)	Reserved
110 (6)	Illegal Lower Machine/ASMD Transfer Size Detected
111 (7)	ASMD Lower Machine Command Parity Error

FIG. 33
PART II